

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Jiang et al.

Serial No.: 09/483,712

Filed: January 14, 2000

For: CHIP-SCALE PACKAGES HAVING
ENCAPSULATED CARRIER BONDS (as
amended)

Confirmation No.: 8743

Examiner: M. Warren

Group Art Unit: 2815

Attorney Docket No.: 2269-3815.1US
(98-0670.00/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 29, 2003
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Leah J. Barrow

Name (Type/Print)

REPLY TO ORDER RETURNING UNDOCKETED APPEAL

ATTENTION: BOARD OF PATENT APPEALS AND INTERFERENCES
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sirs:

Pursuant to the Order Returning Undocketed Appeal mailed December 19, 2003, Appellants/Applicants submit herewith a **Corrected Appendix A** to replace the defective Appendix A attached to the Appeal Brief filed May 27, 2003. Please note that the attached **Corrected Appendix A** incorporates the wording added to Claim 1 by Amendment filed March 27, 2002, which wording was previously inadvertently omitted.

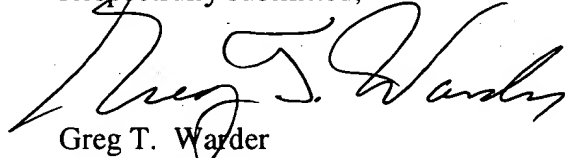
Appellants/Applicants apologize for any inconvenience caused by the omission and appreciate the Board bringing it to our attention.

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Serial No. 09/483,712

Should the Office determine that additional issues remain which might be resolved by a telephone conference, you are respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Greg T. Warder", written over a horizontal line.

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CORRECTED APPENDIX A
(to Appeal Brief filed May 27, 2003)

1. (Previously Twice Amended) A chip-scale package comprising:

- a semiconductor die having an active surface having at least one bond pad thereon;
- at least one conductive trace spaced from said at least one bond pad and having an upper surface and a lower surface, the lower surface of said at least one conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;
- at least one discrete conductive bond member connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;
- at least one carrier bond attached to the upper surface of the at least one conductive trace;
- and
- an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one discrete conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

2. (Previously Three Times Amended) A chip-scale package comprising:
a semiconductor die having an active surface having a plurality of bond pads thereon;
a dielectric element having an upper surface and a lower surface, the lower surface of
said dielectric element attached to a portion of the active surface of said
semiconductor die;
a plurality of conductive traces spaced from said plurality of bond pads, each trace of the
plurality of conductive traces having an upper surface and a lower surface, the
lower surface of each trace of said plurality of conductive traces attached to a
portion of the upper surface of said dielectric element for connecting each
conductive trace of said plurality of conductive traces to the active surface of said
semiconductor die;
a plurality of discrete conductive bond members, at least one discrete conductive bond
member of the plurality of conductive bond members connecting each conductive
trace of said plurality of conductive traces to at least one bond pad of the plurality
of bond pads on the active surface of said semiconductor die;
a plurality of conductive carrier bonds, at least one carrier bond of the plurality of
conductive carrier bonds disposed on the upper surface of each conductive trace
of said plurality of conductive traces; and
an encapsulating material disposed about at least portions of said semiconductor die, said
dielectric element, said plurality of conductive traces, said plurality of discrete
conductive bond members and a portion of each carrier bond of said plurality of
conductive carrier bonds.

3. (Original) A chip-scale package as in claim 2, wherein said dielectric element
includes an adhesive-coated polyimide tape.

4. (Original) A chip-scale package as in claim 2, wherein said dielectric element
includes a polyimide film.

5. (Original) A chip-scale package as in claim 2, wherein the upper surface and lower surface of said dielectric element are attached respectively to a portion of the lower surface of each conductive trace of said plurality of conductive traces and a portion of the active surface of said semiconductor die connecting portions of said plurality of conductive traces and portions of said semiconductor die.

6. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive traces comprises a plurality of lead fingers.

7. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive traces comprises a conductive metal.

8. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises a conductive metal.

9. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises bond wires.

10. (Original) A chip-scale package as in claim 9, wherein said bond wires comprise gold or aluminum.

11. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises TAB bonds.

12. (Previously Twice Amended) A chip-scale package as in claim 2, wherein said plurality of discrete conductive bond members comprises thermocompression bonds.

13. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds includes metal.

14. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds is selectively located on the upper surface of said plurality of conductive traces forming an array.

16. (Previously Amended) A chip-scale package as in claim 2, wherein said plurality of conductive carrier bonds comprises solder balls.

17. (Original) A chip-scale package as in claim 2, wherein said encapsulating material comprises a substantially non-conductive material.

18. (Original) A chip-scale package as in claim 2, wherein said encapsulating material comprises a material having a low modulus of elasticity.

19. (Previously Amended) A chip-scale package as in claim 2, wherein each conductive carrier bond of said plurality of conductive carrier bonds further comprises an upper portion and a lower portion, said lower portion of a conductive carrier bond attached to the upper surface of a conductive trace of said plurality of conductive traces.

20. (Previously Amended) A chip-scale package as in claim 19, wherein said encapsulating material is disposed about the lower portions of said plurality of conductive carrier bonds.